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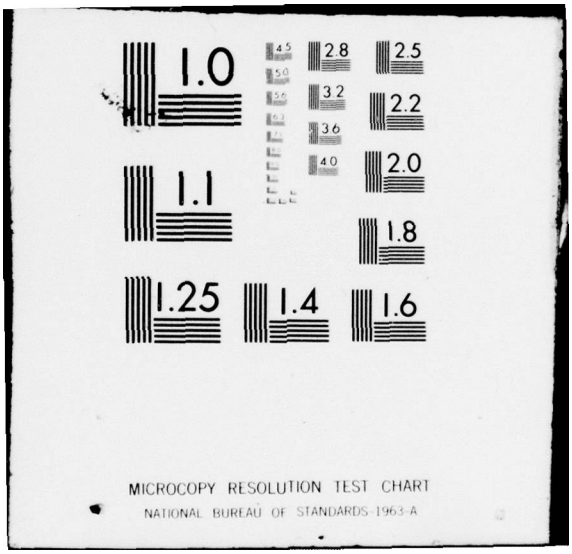
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A simple analytical expression is derived for charge retention in MNOS memory devices assuming that retention loss is limited by Frenkel-Poole release from monoenergetic traps. This model shows that charge retention becomes eventually independent of the initial charge distribution. Experimental data obtained at elevated temperatures confirm this model and provide a trap depth of 1.5 eV, Frenkel-Poole coefficient of about $6 \times 10^{-4} cm^{1/2} V^{-1/2} eV$, and effective escape attempt rate factor of $1.2 \times 10^{8} sec^{-1}$.

The charge versus centroid relationship is determined by staircase charging, in which a sequence of identical pulses is applied, the memory device is returned to flat-band condition after each pulse, and the subsequent pulse is superimposed on the flat-band voltage corresponding to the accumulated memory charge distribution resulting from the preceding pulses. Staircase patterns of accumulated negative charge and of device voltage are analyzed, and effects arising from back-tunneling and leakage currents are identified. The data indicate participation by holes as well as by electrons in charge transport through the dual dielectric at positive gate biases.

CONTINUED ON PAGE 73

CHARGE STORAGE, RETENTION AND ENDURANCE

IN MNOS DEVICES

FINAL REPORT

K. LEHOVEC

JUNE 10, 1979

U.S. ARMY RESEARCH OFFICE

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CONTENTS

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CHIH-HONG CHEN	GRADUATE STUDENT *
SHI-TRON LIN	GRADUATE STUDENT

* Ph.D. Thesis finished with partial support under this contract.

Now with Rockwell International, Anaheim, Ca.

Technical Progress.

This contract concerned research into the basic phenomena occurring in metal-nitride-oxide-silicon memory devices. The phenomena of interest are: the writing and erasing of memory charge in the dual dielectric; the retention of memory charge; and the loss of retention observed after many alternating write and erase pulses (endurance).

Prior to obtaining this contract we published work on the charge distribution of the memory charge introduced at different temperatures[1], and expanded previous theories on the charge distribution to the case of predominant detrapping[2-4]. This theoretical work was based on single carrier-type (electron) charge motion.

During the first year of this contract we studied the memory charge retention at elevated temperatures[5] and showed that detrapping from deep electron traps is the limiting factor for charge retention after an initial phase limited by back-tunneling. However, we became increasingly aware that one-carrier-type theories are insufficient to fully account for the behavior of MNOS devices, and that improved experimental tools are required to elucidate the more comples relationships to be expected when both electrons and holes participate in charge flow. We devised a new method, namely, staircase charging[6] for charging the dual dielectric, under conditions in which the electric field in the oxide is controlled and known. The method involves the application of a sequence of identical small voltage pulses, continuous sensing of the charge state of the silicon surface by capacitance measurements, a feedback circuit to re-establish a specified charge

state of the silicon surface by applying the appropriate gate bias voltage, and monitoring the charge flow through the external circuit. More recently, we have digitized the feedback circuit and combined the measuring edquipment with a data acquisition system (PDP-11) which regulates the application of the identical voltage pulses, stores the measurement data, and evaluates the data in real time[7]. In the Appendix we describe recent results obtained with the staircase method. Some of these results were presented at the Non-Volatile Memory Workshop held in Monterey during March 1979[8]. Investigation of MNOS devices using the staircase method is continuning under contract DAAG29 - 79-C - 0095.

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APPENDIX

NEW EVIDENCE FOR HOLE INJECTION FROM THE GATE OF MNOS DEVICES

Abstract. Charging of MNOS capacitors and memory charge retention are investigated at constant oxide fields using the staircase charging method[1]. The data indicate participation by holes as well as by electrons in charge transport through the dual dielectric at positive gate biases.

Introduction. When a positive gate voltage pulse is applied to an MNOS device with thin oxide layer, enabling tunneling, the flat band voltage is shifted to a more positive value. Since the flatband voltage derives from the charge distribution in the dual dielectric, weighted by the distance from the gate electrode, the positive flat band voltage shift indicates the addition of a net weighted negative charge. Because of the dominance of the negative charge injected from the silicon, early theories considered only single carrier (electron) transport[2-5]. However, recent experimental evidence reviewed in ref. 6, indicates that hole injection from the gate, while not dominant for charging the dielectric, nevertheless does play an important role in the charging. New data presented in what follows confirms these findings and show that hole injection from the gate is also significant for charge retention.

The following experimental results, obtained on metal -Si_3N_4 - Si structures demonstrated hole injection from the gate by positive gate voltages.

The current through the nitride in samples with Au, Al, and Mg gate electrodes decreases in the sequence Au, Al, Mg,[7] which correlates with the increasing hole barrier height E_V-E_F=1.9, 3.0, and 4.0 eV,

respectively, deduced from photoemission measurements[8]. The larger current with Au electrode (compared to Al electrode) is associated with a less positive flat band voltage shift[9]. This is to be expected, since the negative charge added by electron injection from the silicon is partially compensated by positive charge due to hole injection from the gate.

Direct evidence for hole injection from the gate was obtained by investigating the fraction of the insulator current which crosses from an inversion layer to the bulk silicon[10], or else a junction placed close to the silicon surface ("shallow junction") [11,12]. This current is due to carriers which enter the silicon from the dielectric and have the polarity of the carriers in the bulk silicon substrate. It was found that the hole-to-electron current ratio is about 0.4 and nearly independent of the total current through the dielectric over a range of six orders of magnitude. For negative gate voltages the entire current through the dielectric appears to be carried by holes, i.e., there is no significant electron injection from the gate electrode.[10-12]

Charge centroid measurements have shown that, under equivalent condition, holes injected from the silicon by negative gate pulses penetrate more deeply into the nitride than do electrons injected by positive gate pulses[13].

The key issue for understanding charge transport through the dual dielectric are the questions of whether the current is injection-limited or bulk-limited, which fraction of the current is caused by electrons and holes, respectively, and where recombination of electrons and holes occurs[14].

The Frenkel-Poole mechanism often invoked in the evaluation of MNOS experiments applies to charge transport through the bulk of the nitride[15]. As such, it will be governed by the average nitride field, in a first order approximation. On the other hand electron or hole tunneling from

the silicon through the oxide, at positive, or, respectively, negative, gate voltages are injection processes which are strongly dependent on the electric field in the oxide. This suggests experimental conditions in which the oxide field remains fixed at a controlled value. We may then compare, e.g., the steady state current as a function of oxide field and of average field in the nitride with theoretical expectations.

We have applied the previously described staircase charging method[1,16], to obtain charging, charge retention, and steady state current data under controlled oxide field conditions. These results will be described in what follows and interpreted in terms of hole injection from the gate electrode.

Sample Structure and Test Method

We investigated an MNOS capacitor consisting of n-type bulk silicon covered with a 22A° thick SiO_2 layer, on which a 420A° thick Si_3N_4 layer was deposited by low pressure chemical vapor deposition at 700°C. The aluminum gate electrode area was 6.25×10^{-4} cm^2.

A sequence of voltage pulses of alternating polarity was applied to the sample to obtain a reproducible starting condition[17]. The polarity of the final pulse determined the initial flat band voltage. At the negative pulses the sample was illuminated with a He-Ne laser pulse to accelerate the establishment of the inversion charge and to prevent thereby the voltage drop across a deep-depletion layer. The device was charged, or discharged, from the initial state by the staircase method[1,16], illustrated in Fig. 1. A series of pulses of equal height V_p and duration t_p is applied to the gate of the MNOS capacitor. The capacitance is measured between pulses,

and the bias voltage is changed until flat band capacitance is reached. Restoring flat band may require one or a few feedback cycles, each of duration $t_L \simeq 4ms$. The rest period between pulses is thus not a constant, but at most a small multiple of t_L. Since the pulses are always applied at flat band, the oxide field is fully determined by the pulse voltage, V_p, and by the oxide and nitride capacitances:

$$E_{OX} = C_N V_P / (C_{OX} + C_N) t_{OX} \qquad (1)$$

On the other hand, the average nitride field during the pulse is determined by the sum of the flat band voltage V_{FB} and the pulse voltage V_P:

$$\langle E_N \rangle \simeq C_{OX} (V_{FB} + V_P)/(C_{OX} + C_N) t_N \qquad (2)$$

In addition to measuring the difference between flat band voltage before application of a pulse and the re-established flat band voltage after application of a pulse, we also measure the corresponding charge ΔQ flowing through the external circuit. This charge has crossed the silicon-silicon oxide interface, since the charge in the silicon has not changed. Negleting charge change in surface states, and within the thin oxide film, we identify ΔQ with the charge injected into the nitride. For sufficiently short pulses and small voltages this injected charge does not modify the field distribution in the dual dielectric significantly, so that the oxide field during a pulse remains practically unchanged. Dividing this charge by the pulse duration then provides the "oxide current".

After many charging pulses a stationary value of flatband voltage and of oxide current is obtained. These stationary values do not depend on the initial state of the sample before the staircase pulsing, and are independent of pulse duration for pulses longer than a certian value.

The stationary oxide current is the steady-state current through the dual dielectric, since the fraction of injected charge which leaks back to the silicon during the rest period between pulses is being replenished by injection during the pulse, and thus cancels in the total charge increment flowing through the external circuit.

We have also studied the decay of flat band voltage at constant oxide fields by the staircase method using the following procedure: The sample was first charged to a large positive flat band voltage by applying a large positive gate voltage. After removal of that voltage flat band was established and maintained by the capacitance sensing and digital feedback circuits[16] and a sequence of small, fixed positive voltage pulses was applied at flat band as in the staircase charging method. The duration of these voltage pulses, t_p, was choses long versus the rest period t_L.

Experimental Results. Figure 2 shows the buildup of the flat band voltage and of the charge $Q=\int i\partial t$ passed through the external circuit by a staircase charging experiment. Abscissa is the total preceding pulse time, i.e., the rest periods between pulses when flat band is being re-established is not counted. Each data point plotted in Fig 2 by the digital data acquisition system used for the feedback circuit represents one pulse. Flat band voltage approaches a constant value as the number of pulses increases.

The digital system also performs the calculation of $\Delta Q/t_p A$ and of $C_N \Delta V_{FB}/\Delta Q$. The current density $\Delta Q/t_p A$ passes through a minimum and approaches a steady-state value with increasing number of pulses. The interpretaition of the minimum and of other experimental data described in this section will be given in the next section.

The "charging efficiency" $C_N \Delta V_{FB}/\Delta Q$ can be given the following interpretations. If the fraction η of the charge ΔQ crossing the silicon-oxide interface were trapped at the oxide-nitride interface, and the remaining fraction $1-\eta$ were to pass through the gate electrode, as suggested in reference [18] for metal-Al_2O_3-SiO_2-Si structures with tungsten at the SiO_2/Al_2O_3 interface, then $\eta = C_N \Delta V_{FB}/\Delta Q$. (The arrangement of Ref. [18] did not measure ΔQ, while our arrangement does). Or else, if all the charge ΔQ passing the silicon-oxide interface were trapped in the silicon nitride, and the charge already there would not shift during the pulse, then

$$C_N \Delta V_{FB}/\Delta Q = 1-\bar{x}/t_N \qquad (3)$$

where $\bar{x}$ is the centroid of the added charge relative to the oxide-nitride interface and t_N is the nitride thickness. Thus starting from an initially charge-free sample, the centroid vs. charge relation can be derived from

$$\bar{x}\,(Q) = t_n \left[1 - C_N \frac{[V_{FB}\,(Q) - V_{FB}(Q=0)]}{Q} \right] \qquad (4)$$

However, the interpretation of charging efficiency becomes complex if electrons are injected from the silicon and holes enter from the gate. Since such holes trapped in the nitride decrease the flat band voltage, negative charging efficiencies may result and have indeed been observed under certain pulse conditions.

The stationary oxide current which is also the steady-state current through the nitride is plotted against the oxide field and against the average nitride field in Figure 3. Each point of this figure is taken from a staircase charging experiment such as shown in Figure 2 using a different V_p, and charging from an initially negative flat band voltage by positive pulses, and for an initially positive flat band voltage by

negative voltage pulses. The inset in Figure 3 shows the dependence of the steady-state flat band voltage on the oxide field pertaining to the pulse height according to Equation (1). While the steady state flat band voltage increases with positive pulse height, it changes very little with negative pulse height.

The steady state currents for positive and negative pulses are almost identical at the same average nitride field. However, these currents differ considerably from each other when plotted against the oxide field.

Figure 4 shows the decay of flat band voltage of a sample charged to an initially large positive flat band voltage as a function of the heights of pulses applied during the charge retention experiment. One might have expected that these positive pulses further charge the sample, or at least retard its discharge. However, it is seen that small positive pulses actually accelerate the discharge. The steady state value, approached after many pulses, does increase with pulse height, as expected.

Interpretation. It is known that electron injection from the gate is insignificant for negative gate voltages. We attribute therefore the steady state current in Fig. 3 for negative gate pulses to hole injection form an inversion layer on the silicon surface into the nitride by tunneling through the oxide followed by Frenkel-Poole transport through the nitride to the gate electrode. The Frenkel-Poole coefficients $\partial \ln I / \partial \sqrt{\langle E_N \rangle}$ derived from the steady state current vs. average nitride field in Fig. 3 range from 1 to 2×10^{-2} $cm^{1/2} V^{-1/2}$.

The steady state current plotted agianst the oxide field provides the characteristic for holes tunneling through the oxide. The almost constant negative flat band voltage of -11.5V at negative gate pulses is attributed to a positive charge arising from empty electron traps, or else from completely filled deep hole traps. The magnitude of this charge, if located at the

oxide-nitride interface, is 1×10^{13} cm^{-2}, while the trap density is 5×10^{18} cm^{-3} if the charge were distributed uniformly through the nitride. A density of 2×10^{18} cm^{-3} can be derived from the dependence of flatband voltage on nitride thickness reported by Yeargan and Taylor[19].

Considering now the steady state current for positive gate voltage pulses, we notice that this current plotted vs. the average nitride field closely coincides with that for negative gate voltage pulses. Thus the Frenkel-Pooie bulk nitride current is almost independent of the direction of the current for nitride fields of equal magnitudes but opposite polarities. This important observation may mean that bulk nitride current in the steady state is predominatly carried by holes for both pulse polarities.

This interpretation is in general agreement with the model of Svenson[14]. The steady state current plotted vs. the oxide field is much smaller for positive voltage pulses than for negative voltage pulses except at very high oxide fields, where the currents intersect. Shallow junction experiments[11,12] have shown that the oxide current at positive gate voltages is carried by both electons and holes, so that a simple interpretation for the steady state current vs. oxide field at positive gate pulses in terms of single carrier-type tunneling appears inappropriate.

The increase in flat band voltage with positive pulse height suggests that more negative charges are being stored either in the nitride or at the oxide-nitride interface. No saturation of these storage centers is observed for the voltage pulses used in Fig. 3.

We interpret the minimum of the oxide current with increasing number of pulses seen in Fig. 2 as follows: the first few positive pulses inject electrons from the silicon into the oxide-nitride interface, and extract holes from its vicinity. The holes are a residue from the initial biasing condition which terminated with a negative gate voltage pulse.

The electron current decreases for the subsequent few pulses because of increasing occupancy of centers to which the electrons tunnel. The hole current decreases as more holes are extracted. Each of these effects causes a decrease of the charge ΔQ crossing the Si/SiO_2 interface. The net negative charge generated by the injection of electrons and extraction of holes increases the electric field at the gate electrode and enhances hole injection from the gate into the nitride. The oxide current passes through a minimum and increases as increasing numbers of these injected holes reach the oxide-nitride interface, and either pass through the oxide. The promotion of electron current through the oxide by the hole current arriving form the gate at the oxide/nitride interface causes the close coupling of the magnitudes of electron and hole currents through the oxide, independent of the magnitude of the oxide current, as found by the shallow junction experiments[11,12]. We visualize this promotion as arising from holes discharging occupied electron traps at the nitride-oxide interface, and thus permitting electron tunneling to the emptied traps; or else as an enhancement of electron tunneling through the oxide by the strong local field caused by a hole approaching the silicon surface.

The enhancement of the flat band voltage decay by small positive gate pulses shown in Fig. 4 is attributed to increased hole injection from the gate. Thus, while these gate pulses retard back tunneling of electrons to the silicon, they also enhance recombination of the electrons by holes injected from the gate with the latter effect appearing to dominate.

Concluding Remarks. Our staircase charging method has provided the currents through the dual dielectric, both as functions of the oxide field and of the average nitride field. Also, changes in flat band voltage have been quantitatively correlated with the charge passed through the silicon-silicon oxide interface. The results show that hole injection form the gate under positive gate voltage pulses occurs during the negative charge build-up in the dual dielectric.

Finally, it is concluded that electron injection form the silicon into the nitride is promoted by holes arriving at the oxide-nitride interface from the gate.

Appreciation. We like to express our appreciation to Dr. Moiz Beguwala of Rockwell International for supplying samples and helpful discussion.

FIGURE CAPTIONS

1. Gate voltage during staircase charging experiments showing the pulses superimposed on the flat-hand restoration voltage. The oxide field $E_{OX} = C_N V_p / t_{ox} (C_{ox} + C_N)$ is always the same just after application of each pulse.

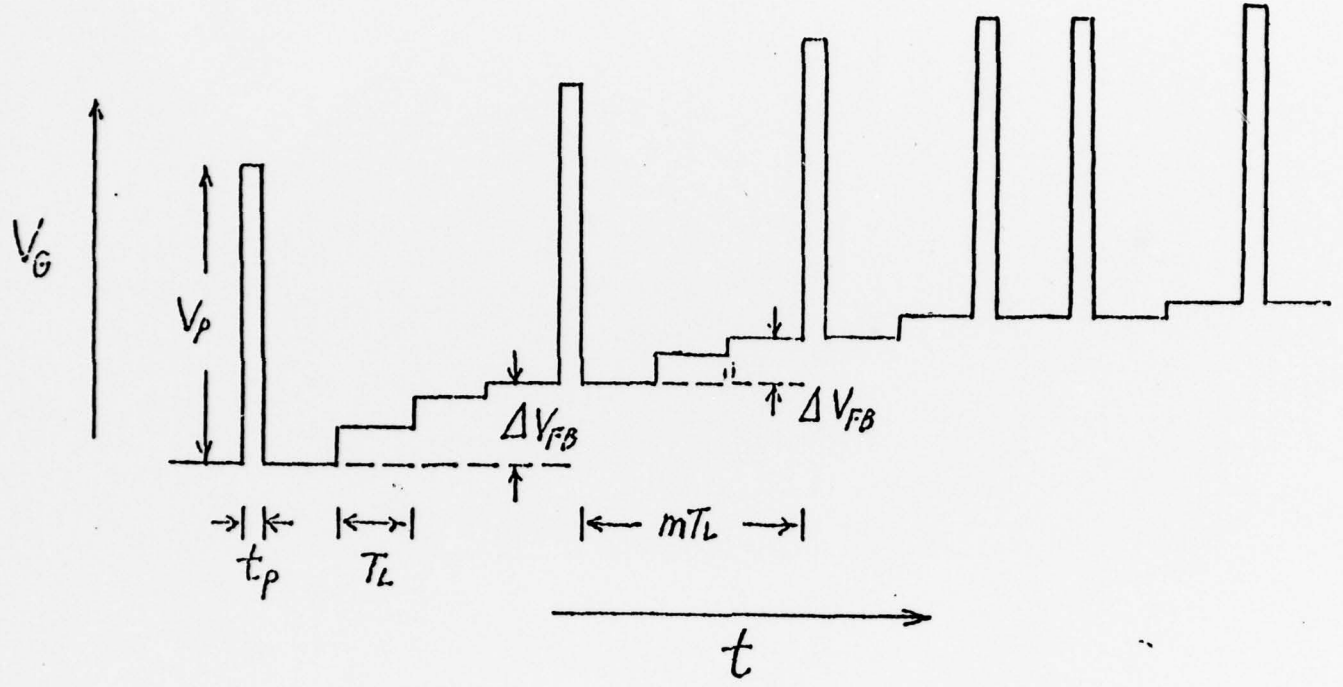
2. Stair-case charging experiment. Each point is the result of an identical pulse V_p=20V, t_p=500 μs. From charge (Q) build-up and flatband voltage (V_{FB}) change we compute the current across the silicon/silicon oxide interface and the "charging efficiency" $C_n \Delta V_{FB} / \Delta Q$.

3. Dependence of steady state currents derived from stair-case charging experiments at different pulse voltages on (a) oxide field and (b) average nitride field for pulses of either polarity. The inset shows the steady state flatband voltage as function of pulse amplitude.

4. Decay of flat band voltage for pulse sequences of different amplitudes applied during the decay while maintaining flat band between pulses.

Pulse duration t_p is long vs. rest period t_L so that the applied voltage is $V_{FB} + V_p$ during most of the decay time plotted as abscissa.

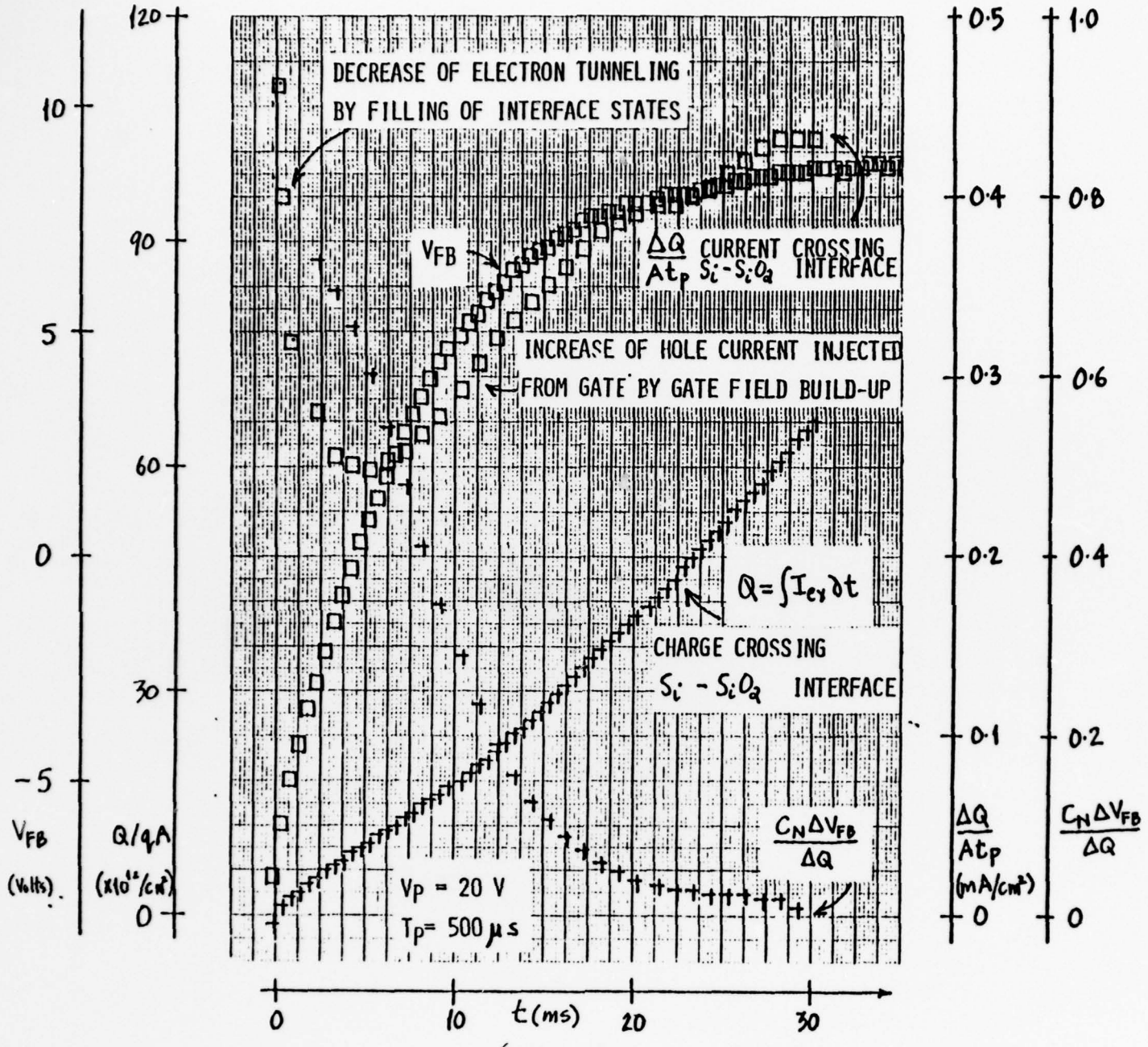
STAIRCASE CHARGING METHOD



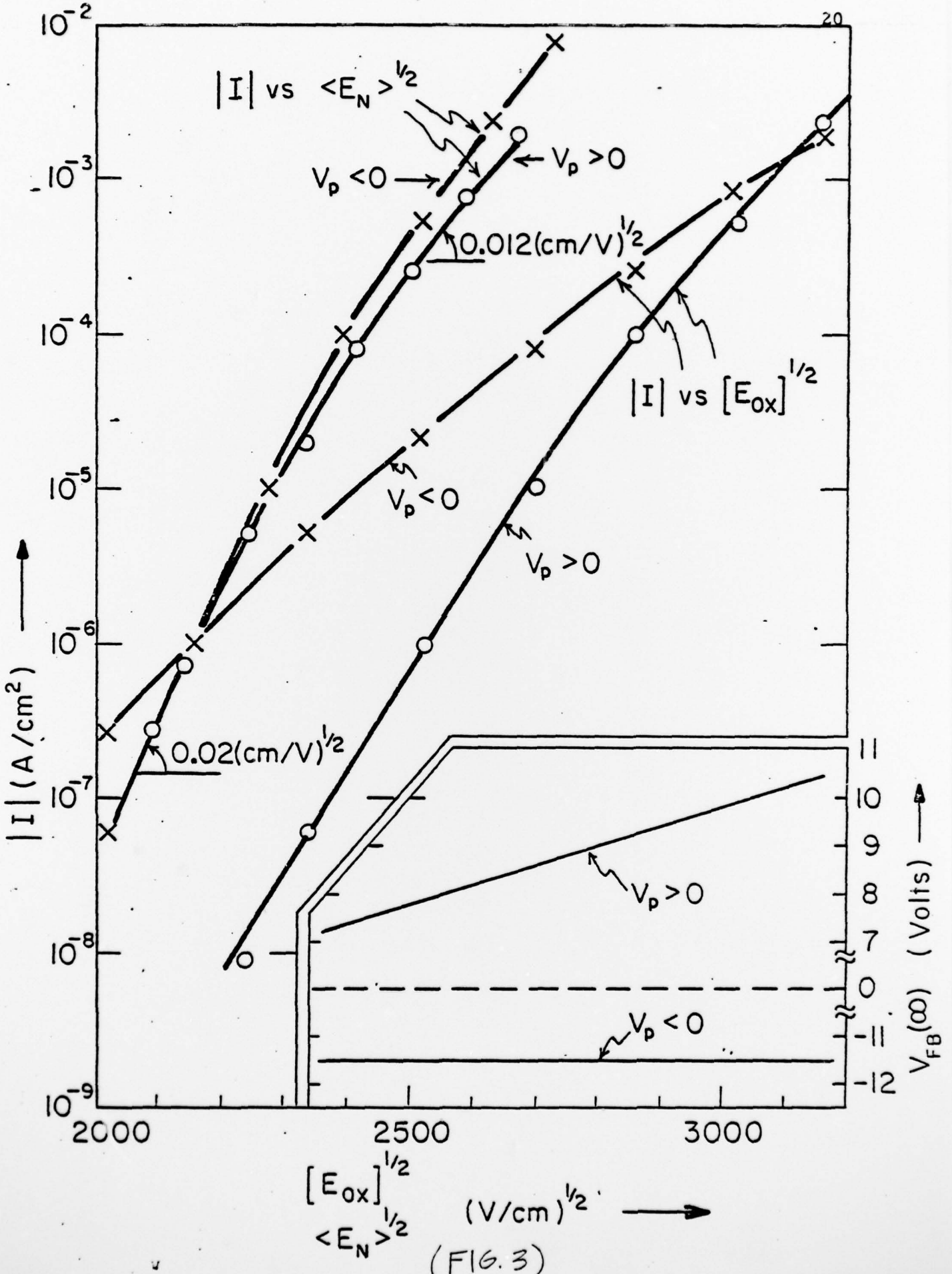
THE OXIDE FIELD IS $\frac{C_N}{C_N + C_{ox}} \frac{V_P}{\epsilon_{ox}}$ JUST AFTER APPLICATION OF EACH PULSE,

$\therefore$ BUT THE FIELD AT THE GATE INCREASES WITH PULSE NUMBER.

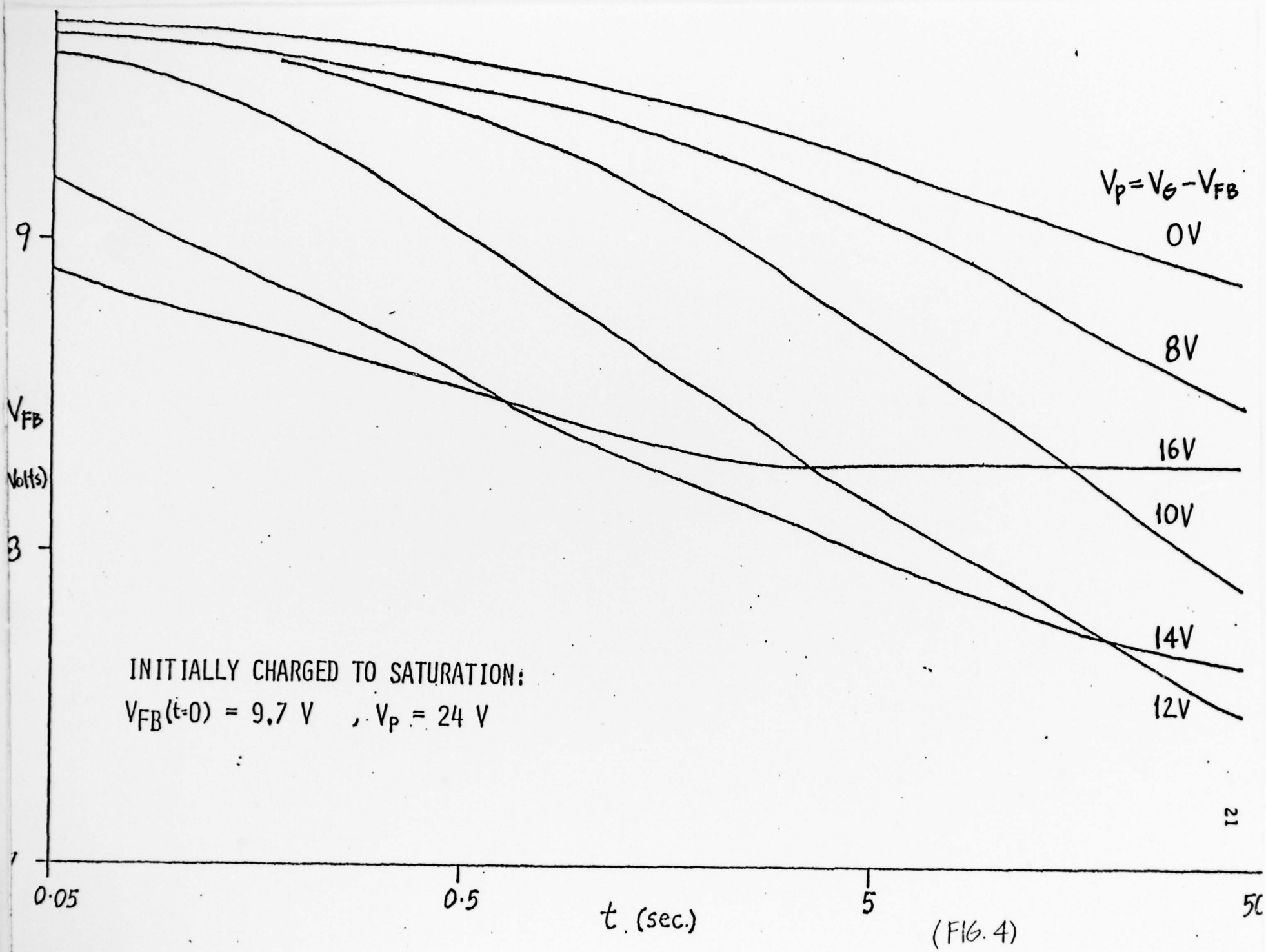
(FIG. 1)


DECREASE OF ELECTRON TUNNELING
BY FILLING OF INTERFACE STATES
V_{FB}
$\frac{\Delta Q}{At_p}$ CURRENT CROSSING S_i-S_iO_2 INTERFACE
INCREASE OF HOLE CURRENT INJECTED
FROM GATE BY GATE FIELD BUILD-UP
$Q = \int I_{ex}\,dt$
CHARGE CROSSING
S_i - S_iO_2 INTERFACE
$\frac{C_N \Delta V_{FB}}{\Delta Q}$
V_P = 20 V
T_P = 500 μs
V_{FB} (Volts)
Q/qA (x10¹²/cm²)
$\frac{\Delta Q}{At_p}$ (mA/cm²)
$\frac{C_N \Delta V_{FB}}{\Delta Q}$
t(ms)
120
10
90
5
60
0
30
-5
0
0.5
1.0
0.4
0.8
0.3
0.6
0.2
0.4
0.1
0.2
0
0
0
10
20
30

(FIG. 2)


|I| vs $\langle E_N \rangle^{1/2}$
$V_p < 0$
$V_p > 0$
0.012(cm/V)$^{1/2}$
|I| vs $[E_{ox}]^{1/2}$
$V_p < 0$
$V_p > 0$
0.02(cm/V)$^{1/2}$
$V_p > 0$
$V_p < 0$
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
|I| (A/cm^2)
11
10
9
8
7
0
-11
-12
$V_{FB}(\infty)$ (Volts)
2000
2500
3000
$[E_{ox}]^{1/2}$
$\langle E_N \rangle^{1/2}$
(V/cm)$^{1/2}$

(FIG. 3)


$V_p = V_G - V_{FB}$
0V
8V
16V
10V
14V
12V
9
3
V_{FB}
(Volts)
INITIALLY CHARGED TO SATURATION:
$V_{FB}(t=0) = 9.7$ V , $V_p = 24$ V
0·05
0·5
5
t. (sec.)

(FIG. 4)

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